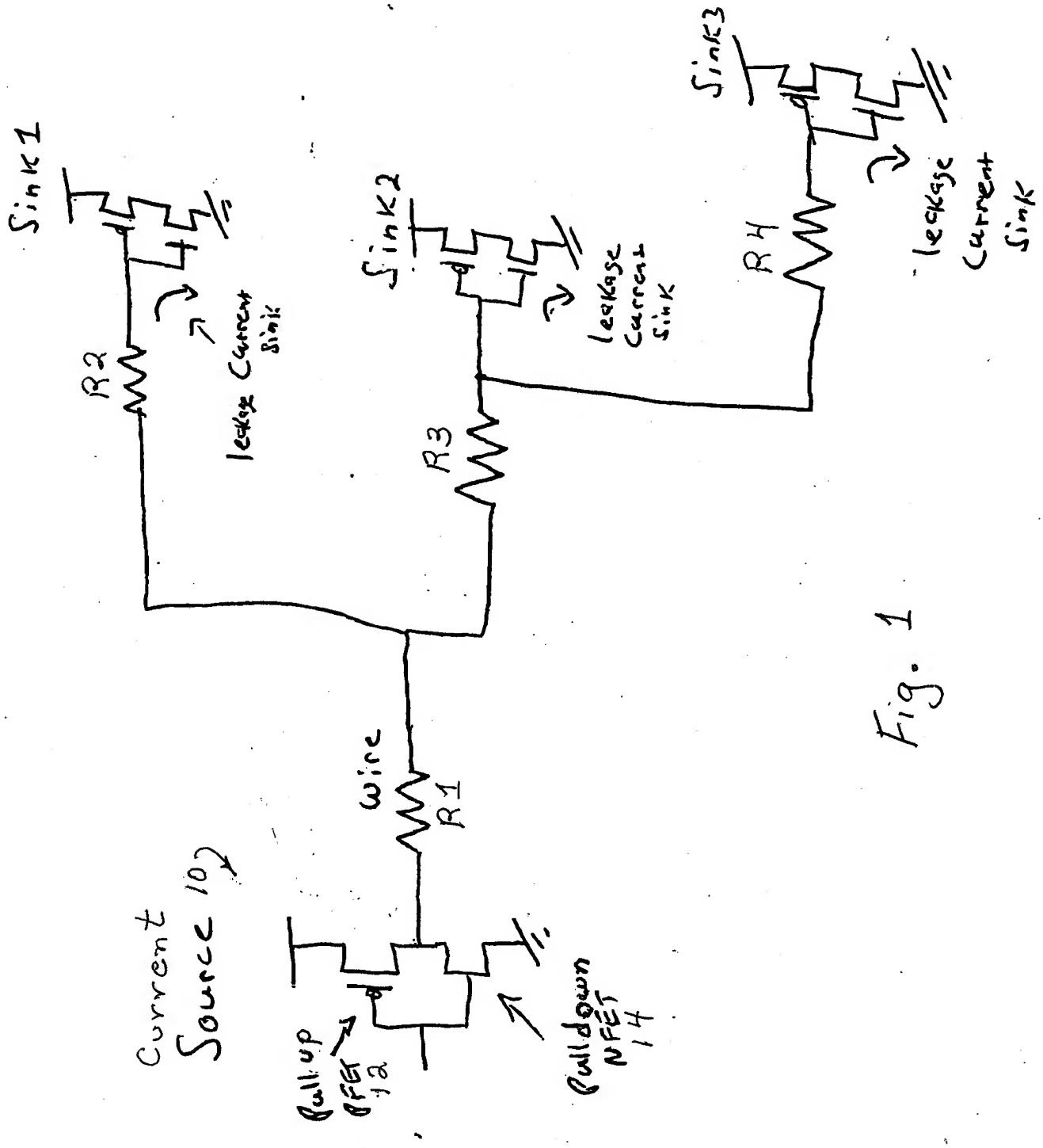
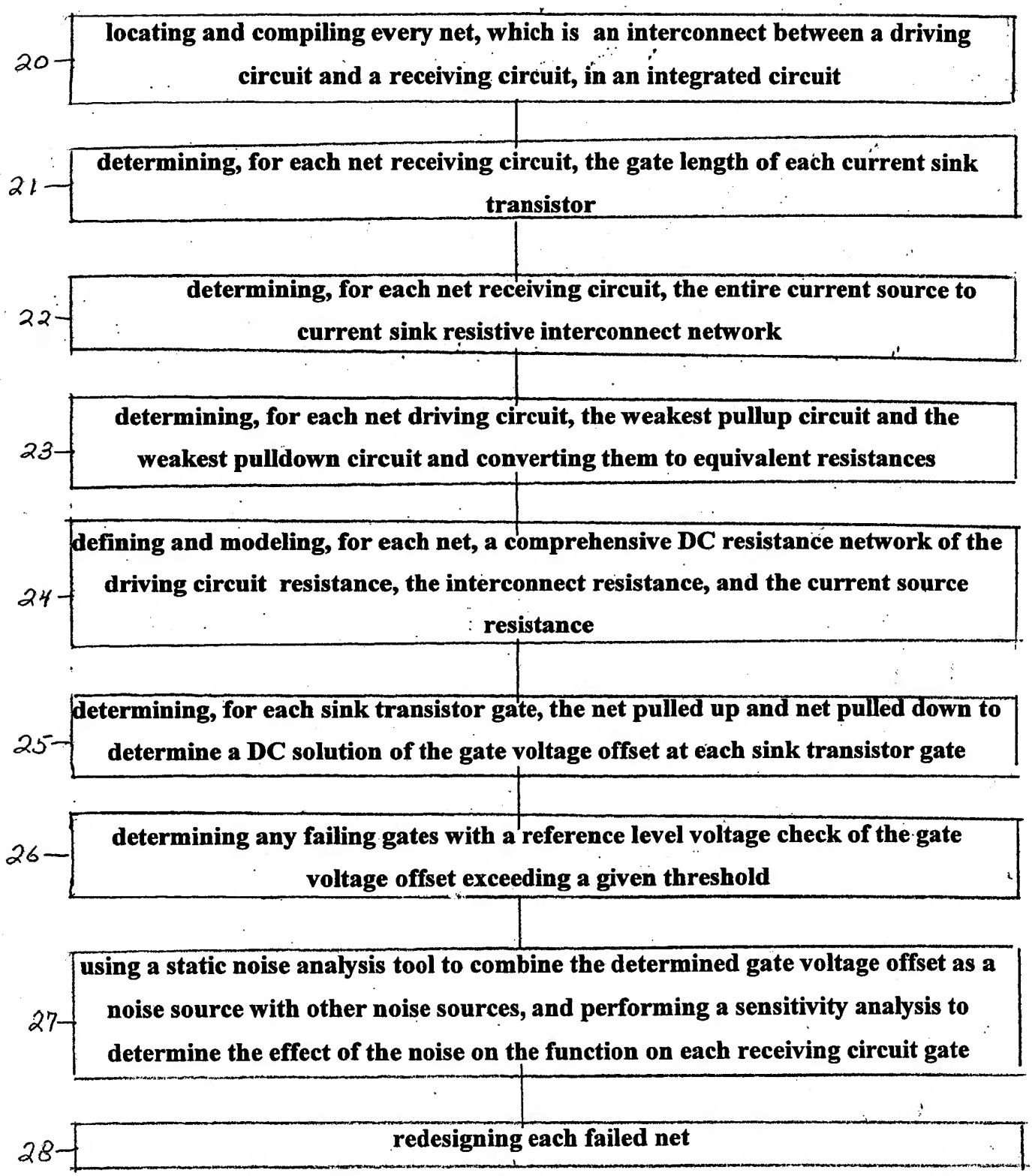

Sink1
Sink2
Sink3
R2
R3
R4
leakage Current Sink
leakage current sink
leakage current sink
wire
R1
Current Source 10
Pull up PFET 12
Pull down NFET 14

Fig. 1

Fig. 2


20
locating and compiling every net, which is an interconnect between a driving circuit and a receiving circuit, in an integrated circuit
21
determining, for each net receiving circuit, the gate length of each current sink transistor
22
determining, for each net receiving circuit, the entire current source to current sink resistive interconnect network
23
determining, for each net driving circuit, the weakest pullup circuit and the weakest pulldown circuit and converting them to equivalent resistances
24
defining and modeling, for each net, a comprehensive DC resistance network of the driving circuit resistance, the interconnect resistance, and the current source resistance
25
determining, for each sink transistor gate, the net pulled up and net pulled down to determine a DC solution of the gate voltage offset at each sink transistor gate
26
determining any failing gates with a reference level voltage check of the gate voltage offset exceeding a given threshold
27
using a static noise analysis tool to combine the determined gate voltage offset as a noise source with other noise sources, and performing a sensitivity analysis to determine the effect of the noise on the function on each receiving circuit gate
28
redesigning each failed net